Unique Wake State Management

&

Extended Power Enablers

for Effective Power Management within US Military Ground Vehicle Electronics and Architecture Solutions

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My background

- Automotive and Military Markets
- Electronics Product Development
- Connected Vehicle Hardware & Software
- Professor of Autonomous / Connected Vehicle Systems; Automated Systems; and Lean Principles and Applications

The Current State

The propagation of electronic solutions to neutralize a threat or add a service within the Vehicle Electronics and Architecture (VEA) for our military ground systems is ever increasing.

Our Focus : Electronic Control Unit (ECU) Development

Many solutions require the addition of another ECU on the vehicle power map and/or diagnostic data bus

The Problem

Improper power state determination and power management techniques in add-on systems induce system vulnerability due to an unanticipated strain on the power management system.

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So how do we create a successful ECU power management solution?

DEFINE THE CURRENT STATE BEFORE ENGINEERING THE SOLUTION.

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So how do we determine the current state of the vehicle architecture interfaces?

Experienced Team of developers map the current state system / processes at a very granular level.

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Value Stream Map of ECU HW/SW

EXAMPLE

Requirement : Need to wake up our diagnostic DIME unit in less than 50ms to be best in class for our product. First vehicle message sent at 100ms.

Developer's Response : After a week of work, the team came back and reported there were 7 software steps and all 7 steps had been optimized such that we could only get down to 95ms for startup time.

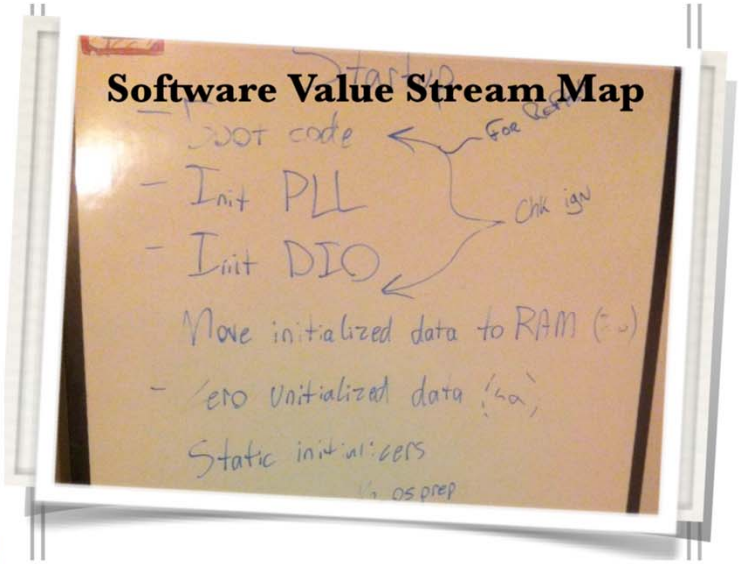
Value Stream Map of ECU HW/SW

Value Stream Mapping with Development Team takes a few hours…

The VSM Results:

The VSM shows 21 steps that occur in software during startup time.

We were only looking at **33%** of the problem!



Granular thinking in regard to hardware and software behaviors by the design team is required.

The Results???

DIME 30 msec start-up achieved!!

So after we have a known current system state mapped what's next?

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Develop architecture of the hardware and software in lock-step to current state system requirements.

What happens when hardware and software are not developed in lock-step?

- OEM example of power dissipation causing failure (Entertainment unit)
- Vehicle to Infrastructure (V2I) hardware designed at different time than software (Safety layer latency)

What happens when hardware and software are developed in lock-step?

Apple iPhone is my favorite example

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So now we have:

Current state mapped 

Software and hardware teams integrated 

Now what?

Now we need to understand **power state scenarios** and their hardware and software interdependencies.

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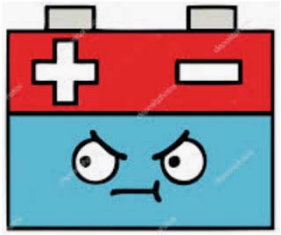
Understanding Power Scenarios

- The power characteristic of most ECUs is understood in steady state power



- *However, the impacts and effects of transitioning between various power states is often neglected in design*.

So HOW do we implement a successful system solution for power management?

Understanding of:

- Typical Power States
- Wake States
- Wake State Management (WSM)
- Extended Power Enablers (EPE)

Typical Power State Scenarios

- Shelf Mode
- Normal Operation
- Peak Power Draw Operation
- Sleep Mode Operation
- Emergency Power Loss

These two scenarios are often overlooked or not fully considered in system design.

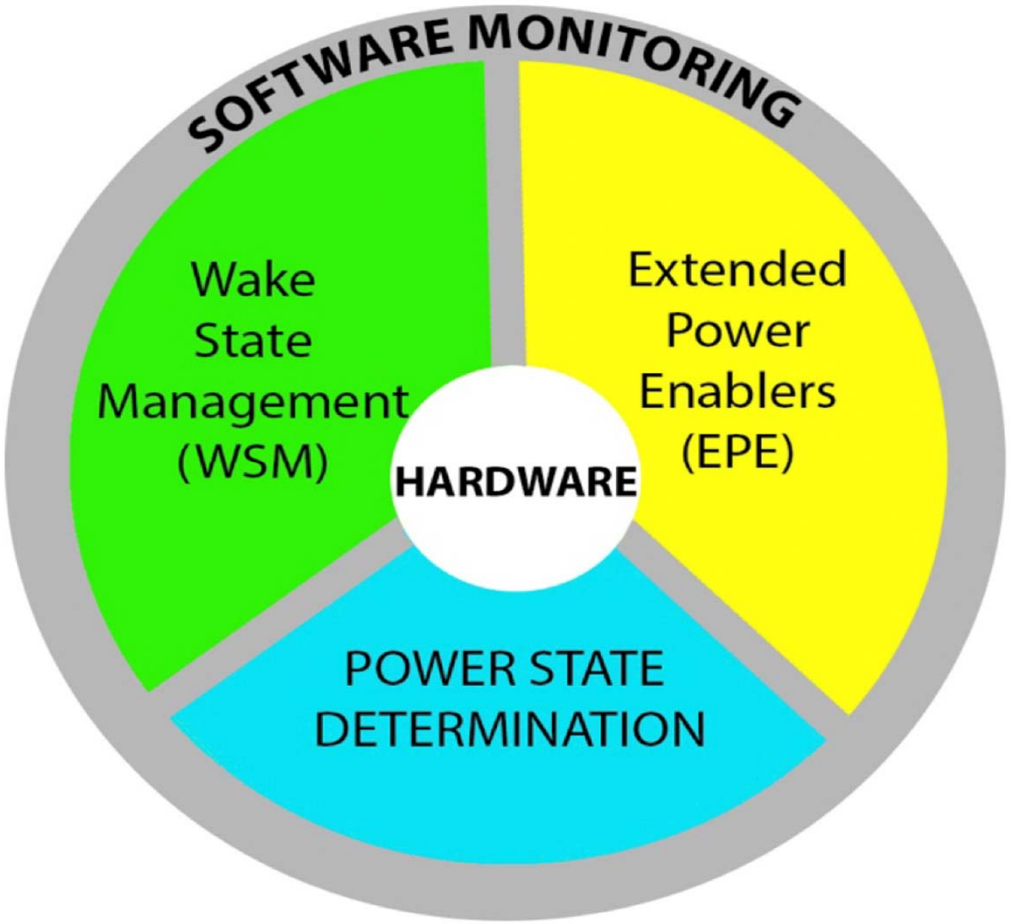
- Sleep Mode Operation
- Emergency Power Loss

Sleep Mode Operation is mitigated by WSM techniques

Emergency Power Loss is assisted by EPEs

So how do these areas help determine the Power State?

Wake State Management (WSM) and Extended Power Enablers (EPE)



WSM and EPEs allow us to map a truly determinate power state at all times!!!

What are Wake States?

- Wake states are system inputs that allow the ECU to transition from zero power or ultra low power mode to full power mode.

Examples of Wake State inputs:

- CAN network bias
- CAN network message transmission
- J1708 Network bias
- Real Time Clock Alarm
- External Digital Input (TTL or equivalent)

Examples of Wake State inputs cont.:

- Analog voltage threshold
  - Switched Ignition
  - Analog input signal from sensor
- Serial Communication Activity
  - RS232, RS422, RS485

Examples of Wake State inputs cont.:

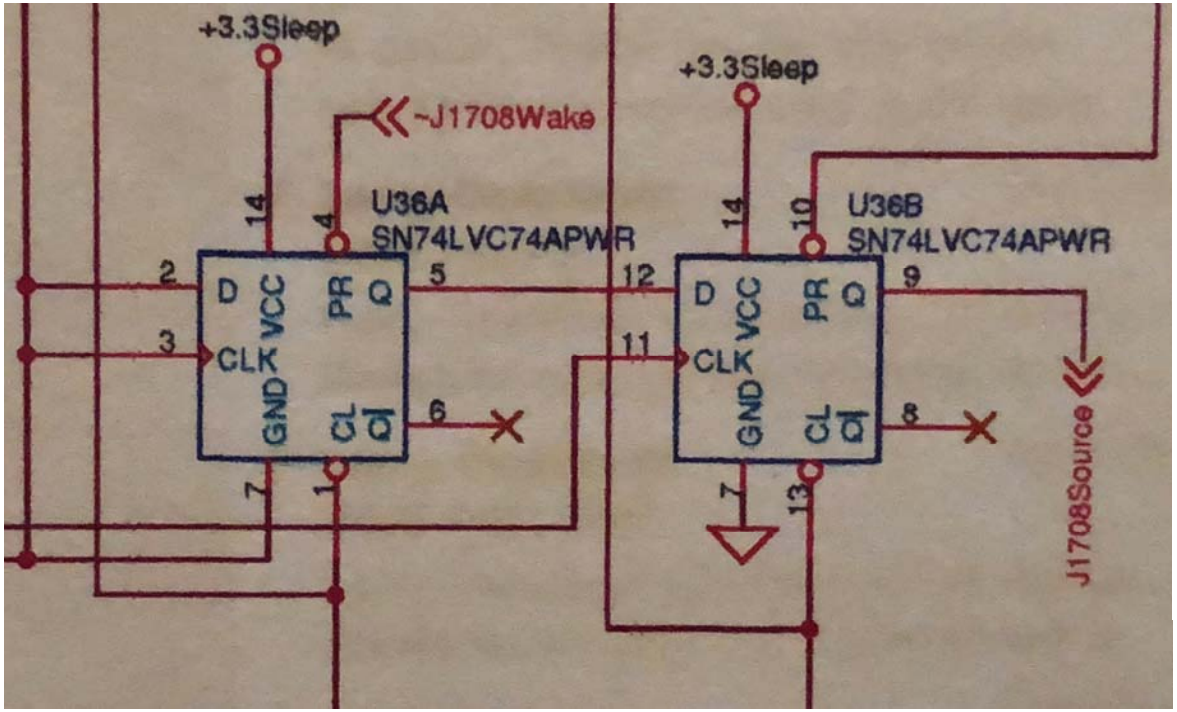
- System Power cycling
- Ethernet activity

What is Wake State Management (WSM)?

WSM ensures configuration and control of power consumption scenarios at all times through identification and management of wake state inputs.

Wake State Management Circuit Example

FLIP-FLOPs are an excellent way to isolate and detect wake states with ultra low power draw in sleep mode.



What are the benefits of WSM?

- State controlled wake scenarios that enable rapid response to wake state inputs.
- Ability to troubleshoot platform issues that occur prior to the first vehicle diagnostic message transmission
- Capture of 100% of vehicle and sensor data under surveillance. We don't lose ANY data!!!

Keys to Wake State Management (WSM) Success:

- Novel low power hardware triggering circuitry (Flip Flops)
- Discrete understanding of software start-up and shutdown conditions (map of current state)
- Controlling power states in a manner that is determinate (Managing Main Micro POR and LVD)

What are Extended Power Enablers (EPE)?

EPEs are hardware and software solutions that enable power to be stored on-board the ECU to be used in the event of loss of system power.

How do EPEs work?

An on-board energy storage device is charged by system power during normal operation, and when a power loss occurs, the ECU has the ability to back feed this stored power into the system to maintain operation in order to properly shutdown the system safely in a defined state.

What are the benefits of EPEs?

- Ability to extend the run time of the system after system power has been either removed or switched off. (tampering, data blast recorder,etc)
- Integrity of the software file system is maintained at all times in a manner that does not corrupt the file system, system operation or any resultant data files.

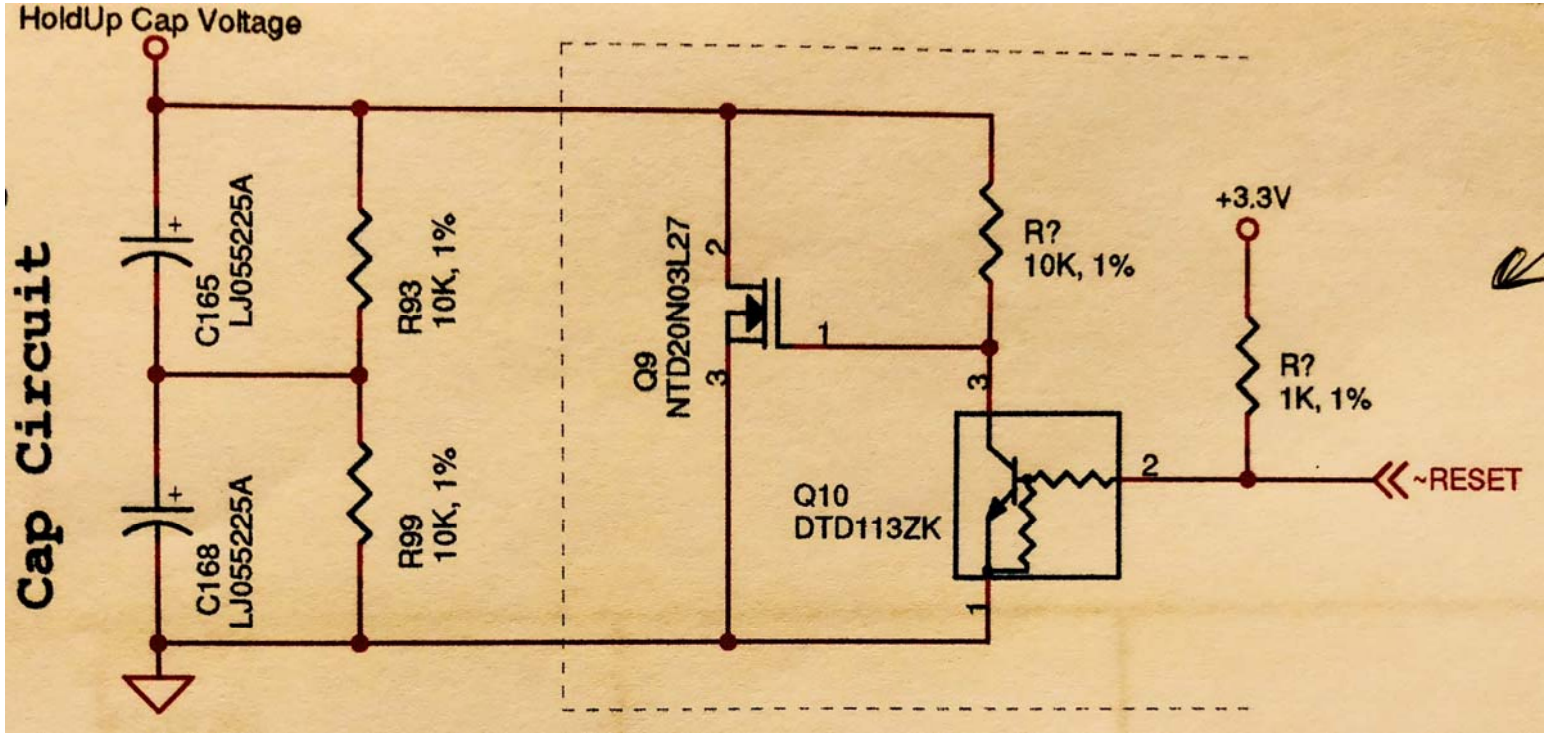
What are the benefits of EPEs? Cont.:

- EPEs ensure power states are determinate at all times which avoids unexpected ECU power draw leading to increased system power vulnerability.
- 100% data under surveillance is captured and managed

What are some examples of EPEs?

- Low Power Unique Wake State Circuitry (flip-flops, state logic,etc)
- Unique energy storage solutions
  (Capacitor backfeed, on-board batteries, etc)
- Effective integration of WSM for low power sleep/wake

Example EPE Circuit : Capacitor Hold-up



What are challenges to EPE implementation?

The microprocessor indeterminate power region in between the Low Voltage Detect (LVD) trigger and the Power On Reset (POR) trigger regions of common 32-bit microcontrollers must be carefully mitigated.

What is the Power On Reset (POR)?

An integrated Power-On Reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. If you fail to manage the shutdown properly your micro could fail to reboot.

What is Low Voltage Detect (LVD)?

The Low Voltage Detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point.

Why do we need to worry about LVD and POR within an EPE solution?

- Once it gets down to that 2.2V range, you get in to a sort of "gray area". There are two voltage levels that are coming in to play: the Low Voltage Detect (about 2.2V) and the Power On Reset (about .3V below the LVD). Once the LVD triggers, you can configure the part to either trigger an interrupt, or assert /RESET. If you get below the POR level, you must assert /RESET (there is no recovery option with the interrupt like there is with the LVD).
- The easiest thing for you would be to assert /RESET once you get down to that 2.2V range, then power back up. Once the voltages get back up to 3.3V, release /RESET and the part should be functional. If you get down to that 2.2V range and do nothing but reapply power, the part will get stuck and not come out of reset, which is the behavior you're seeing.

Warning:

If you get into the indeterminate range of the micro power when backfeeding an EPE solution and power is re-applied by the platform system your device could be left in an indeterminate state.

So how do we avoid killing our microcontroller with an indeterminate state?

When platform power is removed…

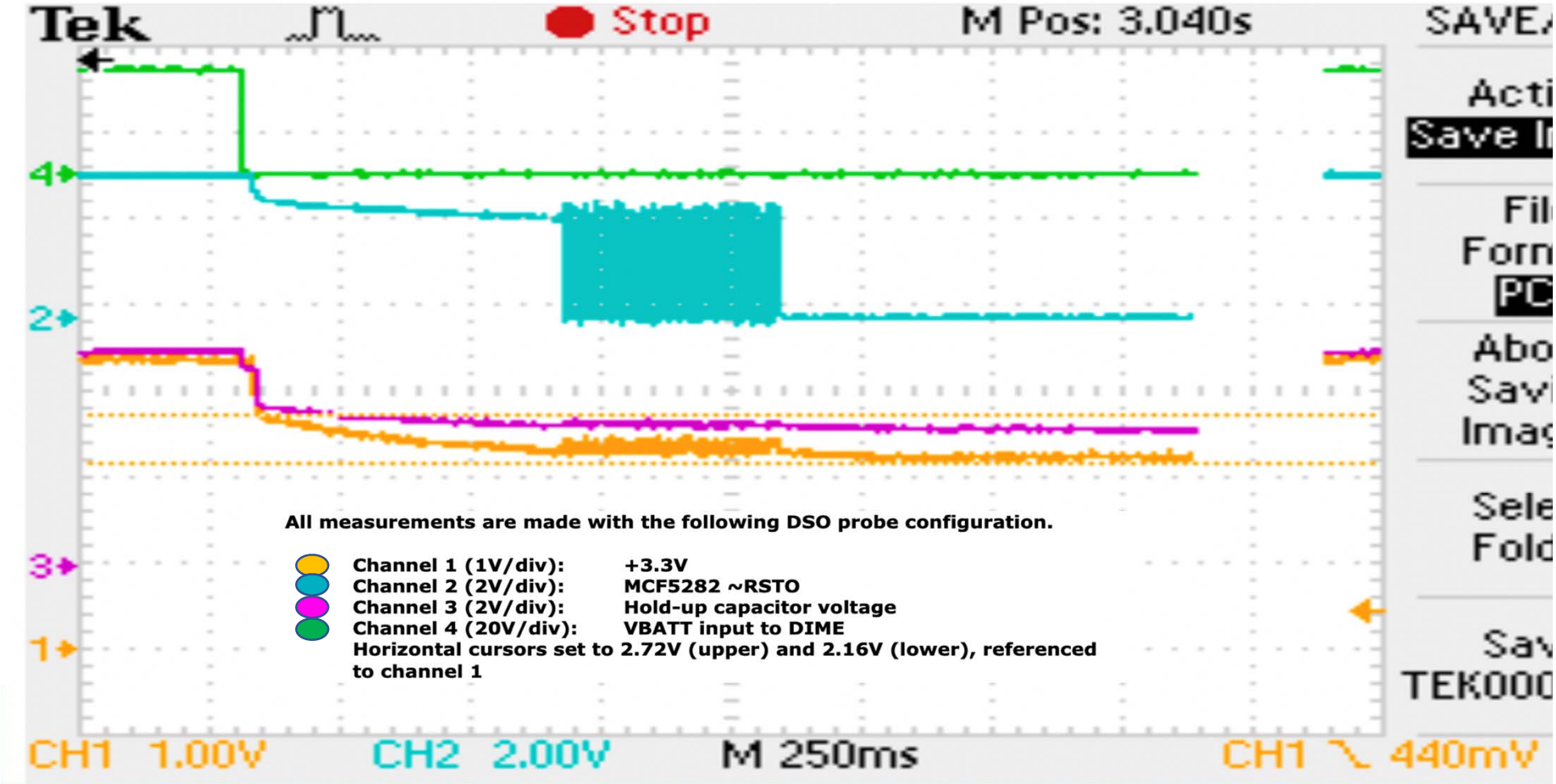
- Real-Time Operating System (RTOS) file system closure occurs
- Power state is set to “Emergency Shutdown”.
- **Rapidly drain the back-feed EPE source of power to zero.**

NEXT SLIDE SHOWS :

RESET CONDITION IN MICRO WHEN LOSS OF PLATFORM POWER DURING EPE POWER BACKFEED EVENT.

Plot 1

MCF5282 is being reset (oscillating) during transitional period defined by horizontal reference cursors. Code will continue to run until reset occurs.



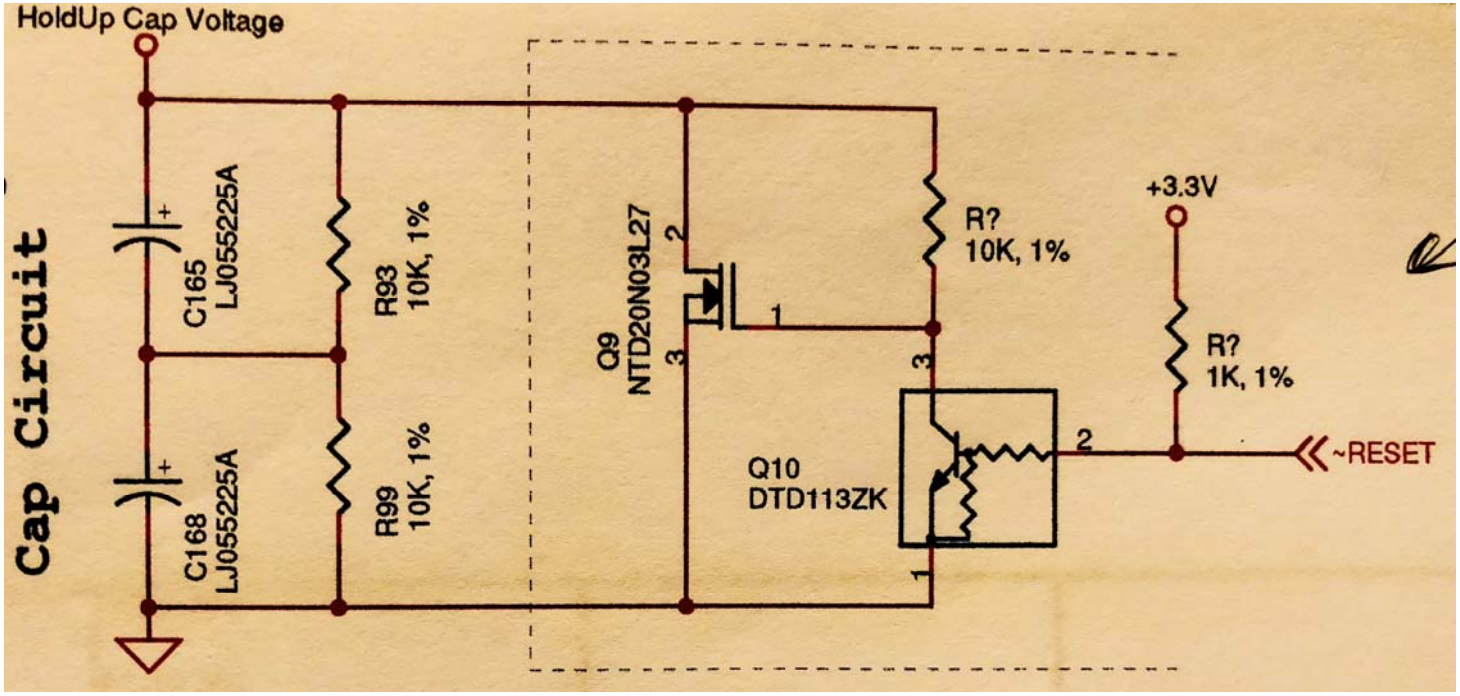
Summary of Emergency Power Loss Scenario to Mitigate Indeterminate State:

- Close files
- Drain back-feed power in a vertical drop or it will linger in the micro indeterminate area and not allow micro to reset to known state when power is re-applied

So how do we remove back-feed power?

(Remember we don't have to drain it to zero, just get it quickly through the POR / LVD range.)

Example EPE Circuit : Crowbar Caps to remove power and enable proper RESET



In Summary

- Wake State Management and Extended Power Enablers allow ECUs to safely integrate new technologies onto legacy platforms without compromising platform power
- Systems approach to design is required and mapping of all known states is key to success.

THANK YOU

Questions???